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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/003,482

12/06/2001

Shmuel Ur

UR=1

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10/19/2006

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EXAMINER

RUTTEN, JAMES D

ART UNIT

PAPER NUMBER

2192

DATE MAILED: 10/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/003,482

Applicant(s)

UR ET AL.

Examiner

J. Derek Rutten

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 July 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8 and 43-65 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8 and 43-65 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is in response to Applicant's submission filed 7/26/2006, responding to the 4/26/2006 Office action which detailed the rejection of claims 1-11, 13-30, and 32-40. Claim 8 has been amended, claims 1-7 and 9-42 have been canceled, and new claims 43-65 have been added. Claims 8 and 43-65 remain pending in the application and have been fully considered by the examiner.

Response to Arguments/Amendments

2. Claims 1-7 and 9-42 have been canceled. New claims 43-65 have been added, and prior claim 8 has been amended to depend from new claim 43. All prior rejections are withdrawn.

3. Applicant suggests at the bottom of page 8 filed 7/2/06, that the Ur reference "gives no hint or suggestion to perform any such test, as is required for coverage analysis, by excluding elements from a software-under-test." However, careful examination of the reference appears to suggest that excluding elements from a software-under-test could be useful. See page 2, 3rd and 4th paragraphs from the top:

...For some Models (e.g. define-use) not all coverage event indicators refer to coverable events... **Knowing in advance which of the event indicators are feasible would make these Models significantly more useful.**

...

For every coverage event indicator [sic] that was not covered via simulation but is coverable, one could use the counter-example mechanism of the Model Checker to provide clues as to **how the test that will cover it should be generated.**
[emphasis added]

As seen from these passages, Ur appears to be interested in performing meaningful tests of software using coverage analysis. Therefore, Applicant's argument that Ur does not suggest performing any test is not persuasive. Also, the suggestion that "Knowing in advance which of

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the event indicators are feasible would make these Models significantly more useful” provides motivation to exclude elements from a software-under-test. Therefore, Applicant’s arguments regarding the Ur reference are not persuasive.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 8, 43, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art of record “Coverability Analysis Using Symbolic Model Checking” by Ur et al. (hereinafter “Ur”) in view of “Unreachable Procedures in Object-Oriented Programming” by Srivastava (hereinafter “Srivastava”).

In regard to claim 43, Ur discloses:

A method for coverability analysis on software under test (SUT), execution of the

SUT generating an outcome, See Ur page 1 paragraph 3:

Every coverage model has a corresponding **coverability model**. A coverability model is defined by creating, for every coverage event indicator in coverage model, a coverability event indicator which is binary function on the state-machine model. The coverability event indicator is true if there exists a test on the state-machine model for which the corresponding coverage event indicator is true. [emphasis added]

the method comprising:

generating rules regarding behavior of the SUT corresponding respectively to coverability tasks for the SUT; See Ur page 1 paragraph 4 lines 3-8:

The second observation is that a state-machine model can be instrumented with control variables and related transitions which, on one hand, retain the original model behavior as reflected on the original state variables, and, on the other hand, can be used for coverability analysis of the model. The analysis is carried out by **formulating special rules** on the instrumented model, and presenting these rules (with the instrumented model) to a Symbolic Model Checker. [emphasis added]

performing a run of a symbolic model checker to test a behavioral model of the SUT, so as to identify uncoverable elements in the SUT and to produce respective results for the rules; See Ur page 1 paragraph 4 lines 6-8:

The analysis is carried out by formulating special rules on the instrumented model, and **presenting these rules (with the instrumented model) to a Symbolic Model Checker** [emphasis added]

computing a coverability metric for the SUT as a function of the results; See Ur page 1 paragraph 1:

...it is shown how a number of **coverability metrics**, corresponding to some commonly-used coverage metrics (statement, multi-condition), **can be implemented** via Symbolic Model Checking (1). [emphasis added]

in response to the coverability metric, identifying a set of the uncoverable elements, such that removal of the set from the SUT is expected to have no effect on the outcome generated by execution of the SUT; See page 2 paragraph 1:

These rules are executed on the Model Checker and a warning on the existence of dead-code is created for every statement that can not be reached.

Note that by definition, dead-code can be removed without affecting the outcome. Also

See Ur page 2 paragraph 3:

...For some Models (e.g. define-use) not all coverage event indicators refer to coverable events... Knowing in advance which of the event indicators are feasible would make these Models significantly more useful.

and performing coverage analysis on the SUT See page 2 paragraph 2:

Coverability analysis can also be used to complement traditional coverage analysis techniques...

Ur does not expressly disclose: *while excluding the set of uncoverable elements from the SUT*. However, Srivastava teaches removing unreachable procedures. See page 356 paragraph 2:

Dead-code elimination [Aho et al. 1988] is a standard compile-time optimization that eliminates useless code in the program: code that is never reached or code that computes a value that is never used in the program. Unreachable procedures are also dead code.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Srivastava's teaching of eliminating unreachable code with Ur's teaching of uncoverable elements in order to make statistics obtained in simulation significantly more useful as suggested by Ur (see page 2 paragraph 3).

In regard to claim 8, the above rejection of claim 43 is incorporated. Ur further discloses: *wherein running the symbolic model checker to test the behavioral model of the SUT comprises: evaluating the respective results so as to determine the truth or falsity of the rules; and generating a list of uncoverable elements responsive to the respective results*. See Ur: "The coverability event indicator is true if there exists a test on the state-machine model for which the corresponding coverage event indicator is true."

In regard to claim 45, the above rejection of claim 43 is incorporated. Ur further discloses: *wherein the set of uncoverable elements comprises dead code*. See page 2 paragraph 1.

In regard to claim 46, the above rejection of claim 46 is incorporated. Ur does not expressly disclose: *wherein the dead code is configured to implement a future modification of the SUT*. However, Srivastava teaches that unreachable code could be a result of code that is available for a future implementation, but that is unused in the current implementation. See page 357 paragraph 1.

6. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ur and Srivastava as applied to claim 43 above, and further in view of the “Background of the Invention” section found on pages 1-13 of the originally filed specification (hereinafter “BOTI”).

In regard to claim 44, the above rejection of claim 43 is incorporated. Ur and Srivastava do not expressly disclose: *wherein generating the rules comprises generating a number of rules less than, by a factor in a range from two to ten, a number of basic blocks in the SUT, and wherein the number of rules is a function of a control-flow structure of the SUT*. However, BOTI teaches model checking optimizations using basic blocks, control flow and domination in terms of “subset cover” algorithms to reduce coverage state space (e.g. page 5 lines 10-19 and page 11 line 33 – page 13). BOTI teaches that basic blocks are made up of statements (page 12 lines 1-4). BOTI further describes the control-flow structure of Fig. 4 in relation to Table II and the subset cover problem on page 13. In this example, the subset cover problem is solved to produce a subset T:

Solving the subset cover problem produces a subset T that covers all the basic blocks in SUT 10, i.e., if every basic block in subset T executes, all basic blocks in SUT must execute. By inspecting the preceding table, it is noted that (B, C) comprise such a

subset, since, if Blocks B and C execute, Blocks A, D, and E must of necessity also execute.

The number of basic blocks in the subset T is less than, by a factor of 2.5, the number of basic blocks in SUT 10. In the case of statement coverage (disclosed by Ur), a reduction in coverage state space using a subset cover algorithm inherently provides a reduction in a number of rules since only a subset of blocks needs to be analyzed. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use BOTI's teaching of the subset cover problem with Ur's teaching of a statement coverage/coverability model. The statement coverage/coverability model contains an event indicator for every statement. The subset cover analysis found in BOTI shows that only a subset of basic blocks requires such event indicators. Thus, the number of rules would be a function of the control-flow structure. One of ordinary skill would have been motivated to reduce the work required of a model checker (BOTI page 5 lines 17-19).

7. Claim 47 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ur and Srivastava as applied to claim 43 above, and further in view of "Compilers: Principles, Techniques, and Tools" by Aho et al. (hereinafter "Aho").

In regard to claim 47, the above rejection of claim 43 is incorporated. Ur and Srivastava do not expressly disclose: *wherein the set of uncoverable elements comprises atomic sub-formulae which cannot evaluate to one of true and false*. However, Aho teaches that an atomic sub-formulae which cannot evaluate to *true* results in dead code.

See page 595. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Aho's teaching of dead code with Ur's uncoverable elements in order to remove dead code as suggested by Aho.

8. Claims 48 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ur and Srivastava as applied to claim 43 above, and further in view of "PC-lint" by Gimpel Software (hereinafter "PC-lint").

In regard to claim 48, the above rejection of claim 43 is incorporated. Ur and Srivastava do not expressly disclose: *wherein the set of uncoverable elements comprises elements having an incorrect variable definition*. However, PC-lint teaches that incorrect variable definitions produce a warning. See page 2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use PC-lint's teaching of incorrect variables with Ur's teaching of uncoverable elements in order to provide a more meaningful analysis of a SUT as suggested by Ur.

In regard to claim 49, the above rejection of claim 43 is incorporated. Ur and Srivastava do not expressly disclose: *wherein the set of uncoverable elements comprises elements having an unused enumerated value*. However, PC-lint teaches that unused enumerations. See page 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use PC-lint's teaching of unused enumerations with Ur's teaching of dead-code in order to make statistics obtained in simulation significantly more useful as suggested by Ur (see page 2 paragraph 3).

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9. Claims 50, 52, 53, 57, 58, 60, 61, and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ur in view of Srivastava and further in view of prior art of record US Patent No. 6,484,134 to Hoskote (hereinafter "Hoskote").

In regard to claim 50, Ur and Srivastava do not expressly disclose:

Apparatus for performing coverability analysis, comprising:

a system memory, which is arranged to contain software under test (SUT), execution of the SUT generating an outcome; and

a computer system processor which is configured to access the memory

However, such an apparatus is disclosed by Hoskote. See Fig. 1. All further limitations have been addressed in the above rejection of claim 43. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Hoskote's apparatus with Ur's method in order to efficiently carry out the method.

In regard to claims 52, 53, and 57, the above rejection of claim 50 is incorporated. All further limitations have been addressed in the above rejections of claims 45, 46, and 8, respectively.

In regard to claim 58, Ur and Srivastava do not expressly disclose:

A computer software product for performing coverability analysis on software under test (SUT), execution of the SUT generating an outcome, the product comprising a computer-readable medium having computer program instructions recorded therein...

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However Hoskote teaches such a computer product. See column 3 lines 58-63. All further limitations have been addressed in the above rejection of claim 1. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Hoskote's product with Ur's method in order to store instructions for a method for easy distribution and archival.

In regard to claims 60, 61, and 65, the above rejection of claim 58 is incorporated. All further limitations have been addressed in the above rejections of claims 45, 46, and 8, respectively.

10. Claims 51 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ur, Srivastava, and Hoskote as applied to claims 50 and 58 above, and further in view of BOTI.

In regard to claim 51, the above rejection of claim 50 is incorporated. All further limitations have been addressed in the above rejection of claim 44.

In regard to claim 59, the above rejection of claim 58 is incorporated. All further limitations have been addressed in the above rejection of claim 44.

11. Claims 54 and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ur in view of Srivastava in view of Hoskote and further in view of Aho.

In regard to claim 54, the above rejection of claim 50 is incorporated. All further limitations have been addressed in the above rejection of claim 47.

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In regard to claim 62, the above rejection of claim 58 is incorporated. All further limitations have been addressed in the above rejection of claim 47.

12. Claims 55, 56, 63, and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ur, Srivastava, and Hoskote, and further in view of PC-lint.

In regard to claims 55 and 56, the above rejection of claim 50 is incorporated. All further limitations have been addressed in the above rejections of claims 48 and 49, respectively.

In regard to claims 63 and 64, the above rejection of claim 58 is incorporated. All further limitations have been addressed in the above rejections of claims 48 and 49, respectively.

Conclusion

13. Applicant's amendment necessitated the new grounds of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

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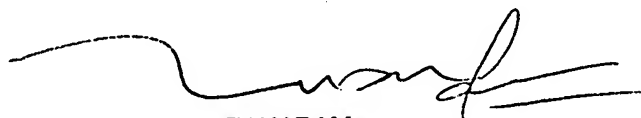
however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. Derek Rutten whose telephone number is (571)272-3703. The examiner can normally be reached on T-F 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571)272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jdr



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SUPERVISORY PATENT EXAMINER